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SPACE LAUNCH SYSTEM PROGRAM (SLSP) INTEGRATED AVIONICS TEST FACILITIES (IATF) VERIFICATION, VALIDATION, AND ACCREDITATION (VV&A) PLAN

REVISION AND HISTORY PAGE

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1.0 INTRODUCTION

The Space Launch System (SLS) Integrated Avionics Test Facilities (IATF) Verification, Validation, and Accreditation (VV&A) Plan presents the approach to be used for the verification, validation, and accreditation for the SLS IATF Hardware (HW), Software (SW), facilities and emulators described in the SLS IATF Development plan (SLS-PLAN-065). The plan addresses the verification and validation of the associated IATF HW/SW, facility, and emulator requirements described in the SLS IATF Requirements Document (SLS-RQMT-066).

The IATF consists of laboratories and emulators designed for supporting the integration and test of the Space Launch System (SLS) avionics and software as outlined in the SLS Integrated Avionics Integration and Test Plan (SLS-PLAN-130). The Avionics System Simulation, Integration, and Support Team (ASSIST) at Marshall Space Flight Center (MSFC) will develop the SLS IATF facilities and emulators. Emulators are HW/SW simulations that represent the SLS Vehicle and are used by external programs to support their development, integration, and testing efforts. The identification of IATF stakeholders that play such an integral role in the VV&A approach in this document are identified in the SLS IATF Development Plan (SLS-PLAN-065).

Accreditation is the official approval by an authorizing agent that a model or simulation is acceptable for use for a specific purpose. Following this definition, the IATF HWIL Simulation will be the only IATF product to receive Accreditation.

The IATF Facilities will be certified in accordance with the SLS IATF Development Plan (SLS-PLAN-065). That plan states that in order for a particular IATF Facility to be used to support formal testing, the facility will need to undergo the process of certification. The facility will be considered certified for use when the Test Readiness Review Board (TRRB) has approved the facility for use in the planned testing.

1.1 Purpose

The purpose of the SLS IATF VV&A Plan is to describe the approach for accomplishing the verification, validation and accreditation of the SLS IATF facilities and emulators. The plan covers the IATF development, integration, and operations and sustainment where the goal is to provide stakeholders, as defined in the SLSP IATF Development Plan (SLS-PLAN-063), with confidence in the execution and credibility of the IATF HW and SW in order to support the analysis and closure of SLS Avionics HW and SW requirements as described in the SLS V&V Plan (SLS-PLAN-009) and the SLS Integrated Avionics Integration and Test Plan (SLS-PLAN-130).

1.2 Scope

This plan is applicable exclusively to VV&A for all SLS IATF HW/SW, facilities, emulators, and associated products produced and delivered by the ASSIST development team at MSFC.

This document is a data managed (Category 2) document used to describe Program Scope defined with SLS Baselined (Category 1) documentation. Work content and organizational

responsibilities described within this documentation are provided to facilitate planning and to familiarize the reader with the interrelationship of activities within the SLS baseline. Specific integrated development agreements in the execution of this document's Program Scope description are defined in the SLS baseline documentation. In the event of an inconsistency of this document with SLS baseline documentation, the Baseline documentation is authoritative. See section 2.0 for guidance on the primary authoritative sources for this Plan.

1.3 Change Authority/Responsibility

The NASA Office of Primary Responsibility (OPR) for this document is ES50, Flight and Ground Software Division at MSFC.

Changes to this document shall be controlled at the OPR level using processes defined by the OPR.

2.0 DOCUMENTS

The agreements that guide and enable the planning content contained in this document are captured in the SLS Program Agreements Document (PAD), SLS-PLAN-186. The integrated development agreements across organizations within the SLS Program are captured in section 8.0 of the PAD and are mapped into the sections shown in Table 2.0-1.

Agreement Area Organization	Section
SE&I	13.1
Multiple Elements	13.2

Table 2.0-1: Integrated Development Agreements

2.1 Applicable Documents

The following documents include specifications, models, standards, guidelines, handbooks, and other special publications. The documents listed in this paragraph are applicable to the extent specified herein.

D201-10082-1	Space Launch System Program (SLSP) Stages Program Master Test Plan (PMTP) Volume 1
GSW-SLS-PLAN-001	IATF Configuration Management (CM) Plan
SLS-PLAN-009	Space Launch System Program (SLSP) Verification and Validation (V&V) Plan
SLS-PLAN-063	Space Launch System Program (SLSP) IATF Software Development Plan
SLS-RQMT-066	Space Launch System Program (SLSP) IATF Requirements Document
SLS-PLAN-065	Space Launch System Program (SLSP) Integrated Avionics Test Facilities (IATF) Development Plan
SLS-PLAN-130	Space Launch System Program (SLSP) Avionics Integration and Test Plan
P2P-00002	Space Launch System (SLS)/Multi-Purpose Crew Vehicle (MPCV)

	Bilateral Exchange Agreement (BEA)
P2P-00003	Space Launch System (SLS)/Grounds Systems Development and Operations (GSDO) Bilateral Exchange Agreement (BEA)
SLS-PLAN-186	SLS Program Agreements Document (PAD)

2.2 Reference Documents

The following documents contain supplemental information to guide the user in the application of this document.

NASA/SP-2007-6105	NASA Systems Engineering Handbook
NPR 7123.1	NASA Systems Engineering Processes and Requirements
NPR 7150.2A	NASA Software Engineering Requirements
SLS-SPEC-032	Space Launch System Program (SLSP) System Specification
SLS-RQMT-095	SLSP Flight Software Requirements Specification
SLS-PLAN-173	Space Launch System Program (SLSP) Modeling and Simulation Plan (MSP)
SLS-PLAN-046	Space Launch System Program (SLSP) Avionics System Simulation and Integrated Test Safety, Reliability and Quality Assurance (SR&QA) Plan
SLS-PLAN-174	Space Launch System Program (SLSP) Integrated Avionics Test Facilities (IATF) Software Assurance Plan (SAP)

3.0 IATF OVERVIEW

The SLSP's IATF will be used to support the SLS Vehicle avionics HW and SW design, development, integration, verification, validation, and certification of flight readiness for the Block 1 launch vehicle. In addition, the IATF will provide emulators to support the external programs as described the Bilateral Exchange Agreements BEA P2P0002, Space Launch System (SLS)/Multi-Purpose Crew Vehicle (MPCV) Bilateral Exchange Agreement (BEA) in Support of Models and Emulations, BEA P2P00003, Space Launch System (SLS)/Grounds Systems Development and Operations (GSDO) Bilateral Exchange Agreement (BEA) in Support of Models and Emulations, as well as to support other element level development and testing.

3.1 IATF Summary

The role of the IATF is to address the requirements of the organizations responsible for performing verification and validation activities as outlined in the SLS Integrated Avionics System Test Plan. Each facility has unique requirements due to the scope of testing and configuration of avionics HW/SW under test. Because many of the operational and functional requirements of each facility are common the verification, validation, and accreditation of those requirements are broken into two major activities - the IATF Hardware-in-the-Loop (HWIL) Simulation System and the IATF Facilities. These requirements are documented in the IATF Requirements Document (SLS-RQMT-066)

3.1.1 IATF Hardware-in-the-loop (HWIL) Simulation System

IATF HWIL Simulation System is comprised of two main Computer Software Configuration Items (CSCIs) and respective HW; the Advanced Real-Time Environment for Modeling, Integration, and Simulation (ARTEMIS) and the Managed Automation Environment for Simulation, Test, and Real-time Operations (MAESTRO). The top-level operational and functional requirements for the IATF HWIL Simulation will be identified in the SLSP IATF Requirements Document.

3.1.1.1 Managed Automation Environment for Simulation, Test, and Real-time Operations (MAESTRO)

MAESTRO is the CSCI that addresses many of the IATF requirements that relate to the test operator functions that control the simulation HW/SW. MAESTRO requirements will be derived through close interaction with each of the IATF users/stakeholders and evolving ARTEMIS requirements throughout the entire SLS development lifecycle.

3.1.1.2 Advanced Real-Time Environment for Modeling, Integration, and Simulation (ARTEMIS)

ARTEMIS is the CSCI that addresses the functions of the simulation that interfaces to the various configurations of the avionics HW/SW under test. ARTEMIS requirements will be

derived from the evolving design of the SLS vehicle avionics and corresponding design constraints (e.g. interfaces, nominal and off-nominal behavior).

3.1.1.3 Special Purpose Hardware

Special purpose hardware relates to the hardware necessary to facilitate the functionality required to drive a specific piece of avionics HW or the ability to reconfigure the HWIL simulation system. Examples of special purpose hardware are cables, special purpose analog/discrete cards, power-break-out-boxes (PBOBs), data-break-out-boxes (DBOBs), Umbilical-break-out-boxes (UBOB).

3.1.2 SLS IATF Facilities

IATF Facilities to be developed are described in the IATF Development Plan and the scope of testing in those facilities is outlined in the SLS Integrated Avionics System Test Plan. The requirements for each facility will be identified in the IATF Requirements Document.

3.1.2.1 SLS Software Development Facility (SDF)

This facility will be used to support the SLS Flight Software (FSW) Development team in developing and testing the SLS FSW. The requirements for the SDF are derived from the evolving SLS avionics design, FSW design, and the FSW test team verification and validation requirements documented in the SLS-RQMT-095, Space Launch System Program (SLSP) Flight Software Requirements Specification. A list of SDF stakeholders includes but is not limited to the following:

- FSW Development Team
- Core Stage Avionics Prime Contractor (e.g. Boeing)
- Guidance, Navigation, and Control (GN&C) Algorithm Development Team
- Mission, and Fault Management (M&FM) Development Team

3.1.2.2 SLS System Integration Test Facility (SITF)

This facility will be used to support the Core Stage Prime in performing integration and avionics box check out activities of the core stage avionics using the SLS Flight computers executing the as-built SLS Flight Software. The requirements for the SITF are derived from the SLS core stage avionics design, the SLS FSW design, and the scope of testing planned by the Core Stage Prime as defined in D201-10082-1, Space Launch System (SLS) Stages Program Master Test Plan (PMTP) Volume 1. A list of SITF Stakeholders includes but is not limited to the following:

- Core Stage Avionics Prime Contractor (e.g. Boeing)
- FSW Development Team
- SLS Stages Element Avionics Insight
- ASSIST Development Team

3.1.2.3 SLS System Integration Laboratory (SIL)

This facility will be used to test the integrated avionics of the SLS Block 1 vehicle. The articles under test will include the core stage avionics, the SLS flight computer flight software (MSFC FSW development team), the booster avionics (single booster flight set), and the core stage engine controllers. In addition, launch control and crew vehicle emulators, provided by respective development program offices, will be used to support the integrated avionics testing described in the Integrated Avionics Test Plan. A list of SIL Stakeholders includes but is not limited to the following:

- Core Stage Avionics Prime Contractor (e.g. Boeing)
- Booster Prime Contractor (e.g. Alliant Techsystems, Inc.)
- Core Stage Engine Prime Contractor (e.g. Pratt Whitney Rocketdyne)
- FSW Development Team
- SLS Integrated Avionics Test Team
- ASSIST Development Team

3.1.2.4 SLS Block 1 Configuration Vehicle Emulators

The ASSIST development team will develop emulators to satisfy external systems development and testing. The specific requirements for each emulator will be derived through interaction with the emulator stakeholder and documented in the IATF Requirements document and respective BEAs. A list of Emulator Stakeholders includes but is not limited to the following:

- Ground Systems Program Office
- Crew Vehicle Program Office
- Mission Operations Program Office
- FSW Development Team
- SLS Program Office
- ASSIST Development Team

3.2 IATF Development Overview

Because the IATF requirements are derived from evolving SLS avionics design specifications and stakeholder needs, the first IATF VV&A activities are scheduled just prior to the first formal testing activity. It is important to understand that VV&A is done incrementally throughout the development schedule because it is driven by the scope in functionality being tested. This approach allows the IATF requirements to reach a higher level of maturity prior to their formal VV&A. Figure 3-1 summarizes the IATF development, VV&A activities (steps 1-8), and the formal test activities.

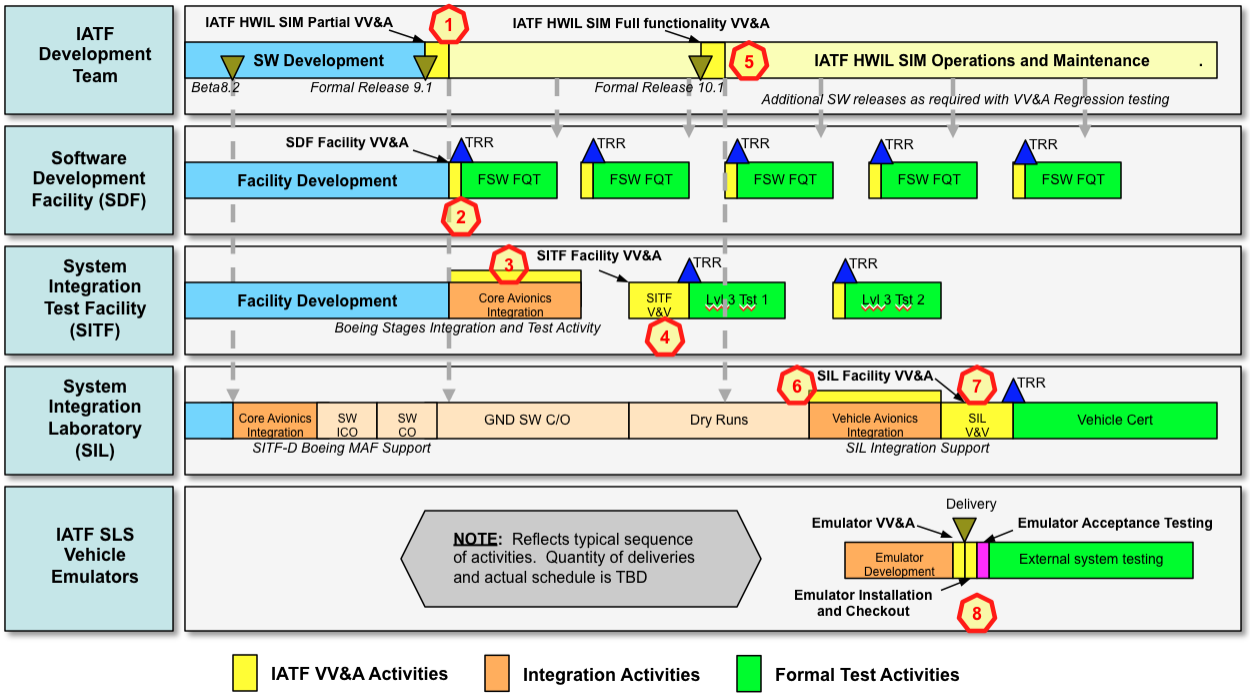

Figure 3-1. IATF Verification Validation Activities

The scheduled IATF HWIL Simulation Formal Release 9.1 will go through a partial VV&A to only include the verification of the functionality required to support testing of the SLS FSW and the Core Vehicle Avionics. Formal Release 10.1 VV&A is intended to address the full functionality of the vehicle. This will require the IATF HWIL Simulation requirements be verified to the maximum extent possible. It should be noted that not all IATF requirements can be fully verified until all the SLS Block 1 Avionics have been fully integrated into the SIL. The following is a brief summary of VV&A activities planned but each will be discussed in the verification, validation, and accreditation sections of this document (each number corresponds to the numbers highlighted in red in Figure in 3-1)

1. Verify the IATF HWIL simulation functionality required to satisfy the first iteration of FSW Flight Qualification Testing (FQT) testing in the SDF and the Core Stage Integration activities in the SITF.
2. Verify the SDF facility, the HWIL simulation hosted on the SDF HW and other SDF requirements required to begin FSW FQT testing. For each FSW FQT test, the SDF facility will go through a delta VV&A activity to ensure the changes implemented since

the last facility VV&A activity have not adversely affected the ability to meet FSW FQT testing requirements. The extent of the VV&A testing will be bounded by the severity and risk associated with the change.

3. For each Core Stage Avionics HW/SW integrated into the SITF, the corresponding HWIL simulation functionality and interface requirements will be verified.
4. Prior to the Level 3 Test 1 activities in the SITF the IATF HWIL Simulation and other facility specific requirements will need to be verified. Like the SDF, for each future formal testing activity the SITF facility will need to go through a delta VV&A exercise.
5. The VV&A activity for closing the simulation functionality requirements required supporting to support the FSW FQT activities in the SDF, the SITF testing, and the SIL integration activities.
6. For each SLS Avionics HW/SW integrated into the SIL, the corresponding HWIL simulation functionality and interface requirements will be verified.
7. The SIL facility requirements will need to be verified. Like the SDF and SITF, for each change in the IATF HWIL Simulation baseline, the SIL facility will need to go through a delta VV&A exercise.
8. The VV&A activity associated with closing the facility specific Emulator requirements prior to shipping to the target facility. Once an Emulator is delivered, the emulator will be installed and checked out prior to the receiving organization performing its acceptance testing.

4.0 IATF VERIFICATION APPROACH

This section describes a verification approach for closing the requirements contained in the SLS-RQMT-066, SLSP IATF Requirements Document, and the derived MAESTRO and ARTEMIS requirements. ASSIST Team roles and responsibilities and associated dependencies on external organizations are described in Appendix B.

Although the focus of this section will be to address the formal closure of the requirements, it is important to understand how the HWIL Simulation development approach and the SW release approach (SLSP IATF Software Development Plan, SLS-PLN-063) establish credibility and confidence in the ability to execute reliably and address the specified requirements.

- The Incremental Software Development Build (defined in the SLSP IATF Software Development Plan) goes through a verification activity to ensure Software Change Requests (SCRs) are implemented correctly. This verification is NOT a verification of IATF, MAESTRO, or ARTEMIS requirements; rather, it only ensures the closure of the set of SCRs assigned to the build. Although each SCR will be traceable to IATF, MAESTRO, or ARTEMIS requirements, the requirements will be changing throughout the development of IATF. Incremental Software Development Build verification artifacts include test plan, test procedures, test data, and test summary report.
- Beta Releases are provided when a stakeholder requests a capability to support a development, integration, or testing activity. Although these Beta releases are provided with limited confidence testing, they allow stakeholders and the development team to assess incremental IATF HW/SW design and implementation, which allows defects to be identified and corrected prior to Incremental Software Development Build verification. In addition, it provides the stakeholders an opportunity to request a modification to the requirements, design, or implementation of the HWIL simulation. These Beta releases will not be used to support SLS formal FSW or avionics requirements. Also, these releases will not be used to verify and validate avionics and software requirements in a formal test environment.
- Throughout the IATF HWIL simulation development, static code analysis results, code-walkthrough data, test reports, SW unit test procedures, data, and documentation will be maintained in SW development folders
- For IATF HWIL HW that is built to support the HWIL Simulation functionality or interface to avionics HW, the ASSIST team built HW (e.g. cables, special purpose discreet and analog cards, PBOB, DBOB, and UBOBs) will be tested and verified as a standalone item or as part of a higher level assembly prior to being included in the formal VV&A testing described in Section 4.1.

The flow of VV&A activities is shown in Figure 4-1 where V&V artifacts are produced throughout development and integration. These artifacts will be described in the tables for each verification activity described later in this section. In addition, these artifacts are then provided as part of the entry criteria at the facility Test Readiness Review. The Test Readiness Review Board (TRRB) will review the VV&A artifacts and certify the facility for formal testing, as described in section 10.0 in the SLS IATF Development Plan (SLS-PLAN-065).

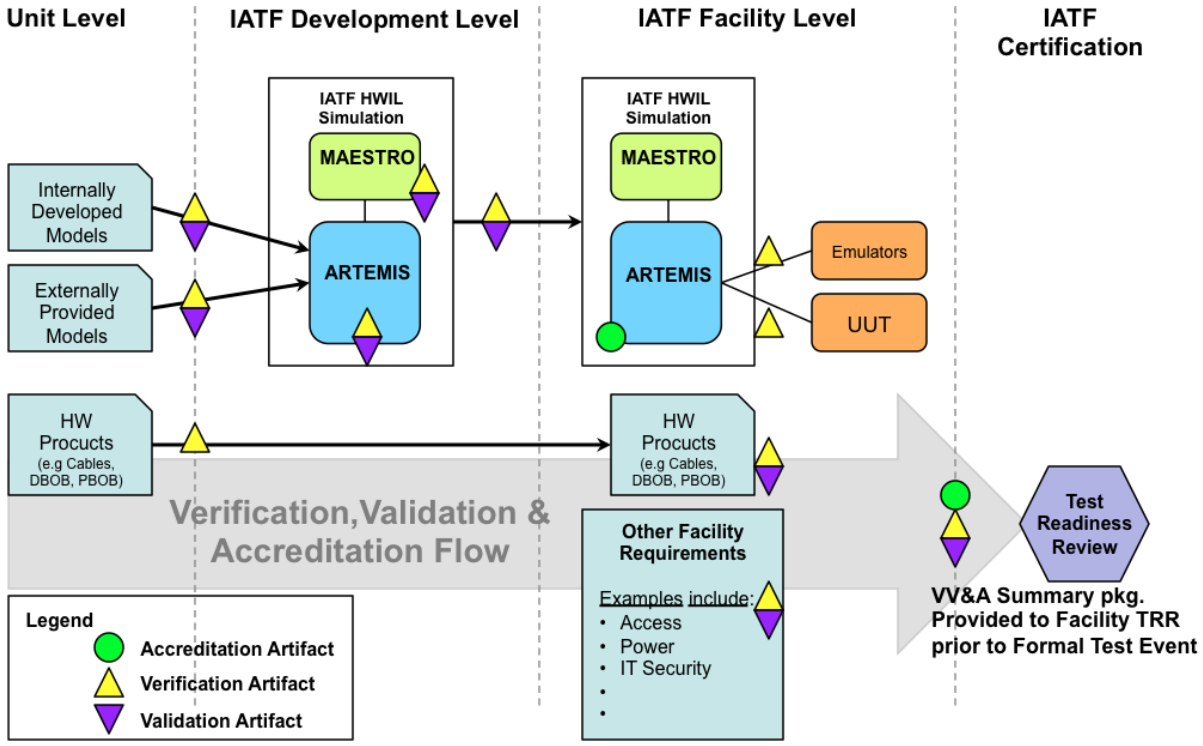

Figure 4-1. IATF VV&A Flow

In general, requirements verification will be accomplished by following these steps:

1. Development of a Verification Cross Reference Matrix and associated Compliance Data List (CDL)
2. Establishing Design Verification Objectives (DVO) that identify verification activities and methods
3. Developing test plans that will ensure each IATF requirement/DVO are addressed
4. Writing associated test procedures
5. Executing tests and analyzing results

6. Writing of verification summary report documenting the closure of all requirements

4.1 DVO Development

As part of requirements management, DVOs will be defined, reviewed, and accepted by IATF stakeholders for each requirement. The process for DVO development including planning and closure of verification activities and associated data schema are outlined in SLS Verification and Validation (V&V) Plan (SLS-PLAN-009). This section is forward work but will address the following:

- What is a DVO
- How the DVOs will be developed
- Who will develop them
- Additional Products produced (e.g. Compliance Data Matrix)
- Participation of QA and S&MA
- Identification of safety issues and ensure and inclusion into the DVO

4.2 IATF HWIL Simulation System Verification

Many of the IATF operational and functional simulation requirements are decomposed into derived requirements for the HWIL Simulation System (e.g. MAESTRO, ARTEMIS, special purpose HW). The HWIL Simulation requirements are derived through active involvement of the stakeholders with the development team and managed through our incremental build process described in the IATF SW development plan.

4.2.1 Formal Release Verification

IATF HWIL Simulation Formal Release verification is the activity of closing the IATF requirements that map to the IATF HWIL Simulation and their derived lower level requirements. Then a detailed test plan will be developed to ensure all IATF HWIL simulation DVOs required for the specific release are satisfied. A set of test procedures will be written to execute the tests specified in the test plan. The IATF SW development approach ensures stakeholder's specific formal release requirements are understood and accepted early enough to allow for the development team to define, design, develop, and test corresponding HW/SW functionality.

As shown in Fig 3-1, IATF HWIL Simulation HW/SW will be verified to the extent possible in the IATF HWIL Development lab; however, certain functionality and interface requirements will not be completely verified until the IATF Simulation HW/SW is integrated with the Avionics HW/SW for a given facility. It is because of this, that many of the verification activities (e.g. 2, 3, 4, 6, 7) described in section 3.2 are planned. The IATF will verify the IATF Simulation

HW/SW functionality and interfaces on the actual hardware used for each facility and will be described in section 4.2.

Verification steps 1 and 5 shown in figure 3-1 will follow the same process of setting up unique test cases in the development labs to ensure the HW/SW functionality and interfaces required to satisfy stakeholder requirements are met. A set of full system level tests will be used to verify that the HW/SW functionality and interfaces are satisfied. These tests will be used again to verify the specific HW/SW used in each facility.

Table 4-1 – Formal Release Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• Validated IATF, MAESTRO, ARTEMIS requirements, • IATF HWIL simulation test plan • Formal release test procedures
Inputs	Baselined IATV HWIL simulation SW and Simulation HW required to support test plan.
Activity	Execute tests in accordance with test procedures. This may require special test configurations.
Outputs	As-run test procedures with notes, test data and logs
Repository	ASSIST Sharepoint
Exit Criteria	Test report verifying the closure of requirements planned for this release

4.2.2 Operations and Maintenance of Formal Releases

Once the IATF HWIL simulation SW is released, Baselined in accordance with the SLSP IATF Configuration Management Plan (GSW-SLS-PLAN-001), problem reports will be generated by the facilities using the IATF HW/SW, which will identify defects that will need to be corrected. Problem reports are generated in accordance with (TBD). The severity of the defect will determine the amount of verification required prior to installing a corrected SW Release. In the case of a minor bug fix, a set of confidence tests will be performed. In the case of a significant design/implementation fix, some of the formal tests used for the formal requirements verification will be examined and adjusted to ensure the IATF HWIL HW/SW fully tests the revised design and implementation. Once fully verified, a new release will be made available to the facilities for installation. The operations and maintenance release will follow the same process as the formal release process described in Table 4-1.

4.3 IATF Facility Verification

Each IATF facility has a specific role in testing the SLS Avionics HW/SW. Each of these roles will require a unique IATF HWIL Simulation configuration.

4.3.1 IATF SDF Verification

The scope of the SDF is to test the FSW executing on the flight computers; therefore, the IATF HW/SW configuration is the HW/SW required to simulate the SLS Vehicle and Avionics such that formal testing of the FSW functionality and interfaces can occur.

Given the required HW/SW functionality and interfaces are verified in the IATF development facilities, the verification in the SDF is limited to Verification Acceptance (VA) testing. This VA testing will be performed by the ASSIST team and can be described as executing system level confidence tests to ensure the HW/SW installed in the SDF are functioning correctly. The following are the artifacts expected to result from this testing:

- Verification Acceptance as-run test procedures
- SDF VA test data, data analysis and test reports (archived at the ESF accordance with the IATF development plan)
- SDF Facility VA memo documenting the IATF Simulation HW/SW satisfied the facility requirements for the set of formal testing planned in the SDF at that time.

Table 4-2 – SDF Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• TBD
Inputs	TBD
Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

4.3.2 IATF SITF Verification

The scope of the SITF is to test the Core Stage Avionics executing flight computers running the FSW; therefore, the IATF HW/SW configuration is the HW/SW required to simulate the SLS Vehicle and the Avionics external to the Core Stage such that formal testing of the Core Stage Avionics functionality and interfaces can occur. There are three principle verification steps to be performed prior to formal testing in the facility; SITF verification acceptance testing, SITF avionics integration, and SITF facility verification.

4.3.2.1 SITF Verification Acceptance Testing

VA testing in the SITF will use the same procedures as the SDF Verification Acceptance testing; however, the amount of IATF HWIL simulation HW will be broader in scope due to the need to

test the Core Stage Avionics and the unique facility requirements. This VA testing performed by the ASSIST team will include the evaluation of the cables, DBOBs, PBOBs, and UBOBs used to interface to the Core Stage Avionics. The verification artifacts produced are the same as those produced in the SDF.

4.3.2.2 SITF Avionics Integration

During Avionics Integration, the Core Stage Avionics will be integrated incrementally where each avionics box Unit Under Test (UUT) integration objectives are tested, evaluated, and closed prior to integrating the next UUT. Prior to each UUT being physically connected to the IATF HWIL HW/SW, the ASSIST team will perform safe-to-mate tests to gain confidence that hardware will not be damaged. Safe-to-mate testing will use the same VA test procedures, but the specific interfaces used to connect to the UUT will be evaluated and a memo written to document the interface requirements were satisfied. Examples of specific interface requirements to verify are continuity, isolation, and hi-pot test performed on cables both pre and post install prior to connecting to avionics HW.

In the SITF, Boeing will be performing the integration of each UUT. This means that Boeing will have its own integration test objectives, procedures, and analysis for each UUT; however, the ASSIST team will leverage Boeing's UUT integration test results to analyze collected data to assess and verify IATF Simulation HW/SW functionality and interfaces. For each UUT a memo will be written to document the IATF HWIL simulation functionality and interfaces were satisfied.

It should be noted that during integration many changes will need to occur in order to successfully integrate with the UUTs; therefore, as described in section 4.2.2, regression testing will need to be performed. Facility operations (Integration schedule) will be critical so it is expected that changes may need to be made in the SITF and then sent back to the IATF development facility for more in-depth regression testing.

The following are the verification artifacts are expected to result from this activity.

- Safe-to-Mate Memo for each UUT documenting the IATF interfaces will not damage the UUT
- Boeing's SITF Integration As-Run Test Procedures.
- IATF UUT interface memo documenting the functionality and interfaces were satisfied for each UUT installed in the SITF.

Table 4-3 – SITF Avionics Integration Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• TBD
Inputs	TBD

Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

4.3.2.3 SITF Facility Verification

Facility verification is done after all UUTs have been successfully integrated into the SITF. For addressing the IATF HWIL simulation requirements, this verification activity follows the same procedures as the VA testing. It is expected that unique Facility requirements will be closed through inspection or special test cases. The following are the artifacts expected to result from this verification activity:

- VA as-run test procedures
- SITF Facility verification VA test data, data analysis and test reports
- SITF Facility verification special test case as-run test procedures, data, data analysis and reports.
- SITF Facility verification memo documenting the Facility Requirements have been satisfied

Any changes to the facility or any part of the UUTs, will require regression testing to verify the changes were implemented as intended without undesired effects.

Table 4-4 – SITF Facility Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• TBD
Inputs	TBD
Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

4.3.3 IATF SIL Verification

The scope of the SIL is to test the SLS Block 1 Integrated Vehicle Avionics; therefore, the IATF HW/SW configuration is the HW & SW required to simulate the SLS Vehicle, external vehicle interfaces, and the sub-system interfaces for each Avionics UUT. There are three principle

verification steps to be performed prior to formal testing in the facility: SIL verification acceptance testing, SIL avionics integration, and SIL facility verification

4.3.3.1 SIL Verification Acceptance Testing

VA testing in the SIL will use the same procedures as the SDF Verification Acceptance testing; however, the amount of IATF HWIL simulation HW will be broader in scope due to the need to test the SLS Block 1 Integrated Avionics and the unique facility requirements. This VA testing performed by the ASSIST team will include the evaluation of the cables, DBOBs, PBOBs, and UBOBs used to interface to the all Avionics UUTs planned for testing. The verification artifacts produced are the same as those produced in the SDF.

4.3.3.2 SIL Avionics Integration

During Avionics Integration, the Avionics UUTs will be integrated one UUT box after another where each UUT's integration objectives are tested, evaluated, and closed prior to integrating the next UUT. Prior to each UUT being physically connected to the IATF HWIL HW/SW, the ASSIST team will perform safe-to-mate tests to verify the IATF HWIL Simulation system will not damage the UUT. Safe-to-mate testing will use the same VA test procedures, but the specific interfaces used to connect to the UUT will be evaluated and a memo written to document the interface requirements were satisfied. Examples of specific interface requirements to verify are continuity, isolation, and hi-pot test performed on cables both pre and post install prior to connecting to avionics HW.

In the SIL, the ASSIST team and each Avionics Prime contractors will have specific integration test objectives, procedures, and analysis for each UUT. The ASSIST team will use these integration tests to analyze collected data to assess and verify IATF Simulation HW/SW functionality and interfaces. For each UUT a memo will be written to document the IATF HWIL simulation functionality and interfaces were satisfied.

Like the SITF, it should be noted that during integration many changes will need to occur in order to successfully integrate with the UUTs; therefore, as described in section 4.1.2, regression testing will need to be performed based on the scope of the change. Facility operations (Integration schedule) will be critical so it is expected that changes may need to be made in the SIL and then sent back to the IATF development facility for more in-depth regression testing.

The following are the verification artifacts expected to result from this activity.

- Safe-to-Mate Memo for each UUT documenting the IATF interfaces will not damage the UUT
- Integration As-Run Test Procedures

- IATF UUT interface memo documenting the functionality and interfaces were satisfied for each UUT installed in the SIL.

Table 4-5 – SIL Avionics Integration Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	TBD
Inputs	TBD
Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

4.3.3.3 SIL Facility Verification

SIL Facility verification is done after all planned UUTs have been successfully integrated into the SIL. For addressing the IATF HWIL simulation requirements, this verification activity follows the same procedures as the VA testing. In addition, the test procedure planned for SIL formal testing will be dry run in the SIL. It is expected that unique Facility requirements will be closed through inspection or special test cases. The following are the artifacts expected to result from this verification activity:

- VA as-run test procedures
- SIL Facility Verification VA test data, data analysis and test reports
- Dry-run SIL formal test procedures and corresponding test data.
- SIL Facility Verification special test case as-run procedures, test data, data analysis and test reports.
- Facility Verification Memo documenting the SIL Facility Requirements have been satisfied

Any changes to the facility, IATF HWIL HW/SW or the SIL UUTs, will require regression testing to verify the changes were implemented as intended without undesired effects.

Table 4-6 – SIL Facility Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• TBD
Inputs	TBD
Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

4.3.4 IATF Emulator Verification

The Emulator requirements are TBD; however, each emulator will go through the same VA process as the SDF, SITF, and SIL only the specific functionality and interfaces required will be evaluated prior to shipping. Once the Emulator is installed in the host facility, the ASSIST team will perform another set of VA test to ensure the system is operating correctly. The specific documentation required for delivery with the Emulator is TBD. The process for release and deployment of the emulators is forward work.

Table 4-7 – Emulator Verification Summary

Participants	ASSIST development Team, QA, S&MA
Entry Criteria	• TBD
Inputs	TBD
Activity	TBD
Outputs	TBD
Repository	ASSIST Sharepoint
Exit Criteria	TBD

5.0 IATF VALIDATION

According to the SLS Program V&V Plan, Validation confirms that the system, when placed in the envisioned environment, will perform its mission as intended. Validation confirms the design is based on the right requirement set and that the system implementation provides the right solution to the stakeholder's needs. ASSIST Team roles and responsibilities and associated dependencies on external organizations are described in Appendix B.

Validation begins during system requirements development and decomposition, and continues throughout integration. Validation ensures delivered products have met the intent of the stakeholders.

A simplified system design validation asks the following questions:

- Will the System, as designed, provide the desired solution?
- Will the System perform its intended mission?
- Is the System as safe as required?

Validation will be an activity performed throughout IATF development in preparation for answering these questions prior to IATF products being used. This validation will support incremental Accreditation discussed in Section 6.0. This section will discuss the context of validation activities with respect to IATF requirements, the IATF HWIL Simulation, and each IATF facilities.

5.1 Requirements Validation

As mentioned in section 3.1 IATF requirements are maturing in step with the SLS Vehicle design and as responsible organizations better define the scope and details of their test requirements. Due to the similarities among the facilities the ASSIST team will be working with all stakeholders to derive requirements that satisfy their needs. The context of IATF requirements validation is to ensure the IATF requirements and associated Design Verification Objectives (DVOs) accurately describe each stakeholder's needs. These requirements are documented in the IATF Requirements Document (SLS-RQMT-066)

The ASSIST team will give all stakeholders the opportunity to review and request the addition, modification, and deletion of requirements throughout IATF development. In addition, the IATF development approach provides opportunities for stakeholders to review the IATF Simulation design and use early prototypes in order to facilitate design and implementation feedback and refinement of requirements.

Stakeholders will participate in the review of the SLSP IATF Requirements document and approval of this document will be considered formal validation of the IATF requirements.

For IATF HWIL Simulation derived requirements, Stakeholders will participate in the ES50 Software Review Board (SRB) review and approval by the SRB will be considered formal validation of the IATF HWIL Simulation requirements.

5.2 IATF HWIL Simulation Validation

We plan use a mix of validation methods defined below (reference Department of Defense's The Office of the Director, Operational Test & Evaluation Joint Accreditation Support Activity Training Document): *Benchmarking, Face Validation, Results Validation, and Sensitivity Analysis* summarized below:

- *Benchmarking* - Comparison of simulation outputs with outputs of another simulation that is accepted as a "standard".
- *Face Validation* - Comparison of simulation design and outputs (under well defined conditions) with the expectations and opinions of subject matter experts (SMEs) in the simulation area of interest.
- *Results Validation* - Comparison of simulation outputs with the results of test measurements made under identical input conditions.
- *Sensitivity Analysis* - Determination of the variation in simulation outputs for measured changes in inputs, functional operations, or other conditions (generally used to supplement other validation methods).

Validation of the IATF does present a challenge because there is no clear accepted standard for comparison (especially for off-nominal conditions) and there isn't any flight test data to validate against. Another challenge is keeping the validation current in an environment where SLS design and implementation changes occur with little regard to the impact to the test community. For the IATF, validation will be accomplished principally through the *Benchmarking* and *Face* validation methods. The following sections will identify the specific methods used for each piece of the IATF HWIL simulation system described in section 3.1.

5.2.1 MAESTRO Validation

Since MAESTRO is principally the test operator interface and has no real world system it represents, validation will be accomplished by using the *Face* validation method where the stakeholders will be the SMEs reviewing the design and associated verification data. Validation of MAESTRO is expected to be very straightforward because stakeholders will be using early prototypes and participating in requirements development. Validation will be documented with a memo documenting the acceptance of MAESTRO for a specific test activity.

5.2.2 ARTEMIS Validation

Throughout IATF development, ARTEMIS validation will follow the *Benchmark* validation method through two stages of activities – model validation and integrated simulation validation. Model validation is the validation of each specific model used within ARTEMIS, which will be used to support the validation of the integrated ARTEMIS simulation. For the purpose of validation, ARTEMIS models will be broken into internally and externally developed models because the validation approach will be slightly different. The intent is to gain confidence and stakeholder approval in the implementation of each model with the understanding that it is a prerequisite to validating the integrated simulation.

The ASSIST team will maintain validation summary data sheets for each model that will provide the model name, objective/purpose, applicability, source, features/limitations, rational for selection, summary of changes made to execute within ARTEMIS, sample plot of comparison data against *benchmark* model or algorithm data, risk identification, and a listing of reference documents. These summary sheets will be updated for each Incremental Software Development Build and formal release and will be included in the validation summary report.

5.2.2.1 Model Validation

First, the ASSIST team will identify Subject Matter Experts (SMEs) for each model to support its validation. The plan is to get their involvement early in the IATF development so they can participate in the review of IATF derived ARTEMIS requirements' DVOs, their associated acceptability criteria, and to influence design and implementation. Since models used within ARTEMIS are either developed by the ASSIST team or they are provided by an external source and then adapted to execute within the ARTEMIS simulation environment, their validation approach is tailored to each model depending on the criticality of the model and risks associated with using the model to perform avionics testing.

5.2.2.1.1 ASSIST Developed Models

For models developed by the ASSIST team, the ASSIST team will compare model results to data produced from the execution of engineering models or test data. The SME for that model will review the comparison analysis in order to ensure the accuracy of the model meets the intended purpose. The validation status of each model will be documented in each model's summary sheet and will be updated as described in section 5.2.2.

For example, for the Main Propulsion System (MPS) model will model fluid rates, valves, and sensors of the SLS Block 1 MPS system. This model will need to be traceable to the actual MPS system design as it evolves to a flight qualified system. The fidelity in which the MPS is modeled is driven by the sensitivity of the control system and will be documented as DVOs and associated acceptability criteria.

5.2.2.1.2 Externally Developed Models

For models developed externally and delivered for use within ARTEMIS, the ASSIST team will adapt the model to execute within the ARTEMIS real-time multi-threaded distributed simulation architecture. These models are to be verified and validated by the provider prior to delivery (including test cases and data used in their validation); the IATF validation of these models will be accomplished by comparing the results of the integrated model against the delivered validation data for comparable test cases. Some variations are expected due to the real-time simulation architecture in which it will have to function. In this case, SME's (typically the model provider) will participate in the development of DVOs and associated acceptability criteria, and review the model's execution results vs. delivered validation data. The validation status of each model will be documented in each model's summary sheet and will be updated as described in section 5.2.2.

5.2.2.2 Integrated Simulation Validation

The integrated ARTEMIS simulation validation is accomplished using the *benchmark* validation method by comparing results against SLS vehicle engineering models (e.g. MSFC developed MArshall Vehicle Representation In C, *MAVRIC*) simulation that is used to develop Guidance, Navigation, and Control (GN&C) algorithms. It is expected that the SLS V&V effort will result in design verification scenarios that will specify the conditions (nominal and off-nominal) the integrated avionics will be evaluated against. These scenarios will be used for comparing the results from both SLS vehicle engineering models and the all-digital configuration of ARTEMIS. SMEs will participate in the development of DVOs and associated acceptability criteria, and review the comparison results with SLS vehicle engineering models. The validation status of integrated ARTEMIS will be documented in an integrated ARTEMIS simulation summary sheet and will be updated as described in section 5.2.2.

5.3 IATF Facility Validation

Facility validation is accomplished by Facility level stakeholders review, prior to it being used, the VV&A artifacts that provide evidence that the IATF facility is capable of supporting the integration or test activity planned. For the first couple of integration and test activities (activities 1&2 summarized in section 3.2), the integration and test activity will be limited based on the capabilities of the UUTs and associated test objectives that mean the VV&A will only cover the necessary IATF functionality required to support that integration/test activity. These VV&A artifacts include: the validation of the facility and IATF HWIL requirements, the IATF verification report for that facility, the IATF HWIL validation report, and IATF HWIL simulation accreditation. This approach will be used for each IATF facility (SDF, SITF, SIL, and Emulators).

6.0 IATF HWIL SIMULATION ACCREDITATION

Accreditation is the official approval by an authorizing agent that a model or simulation is acceptable for use for a specific purpose.

With respect to the IATF HWIL Simulation, the Accreditation organization is the Chief Engineer's Control Board (CECB). The ASSIST team will present the verification and validation summary reports that summarize the artifacts and results for acceptance prior to it being used in a formal test event. It is expected that accreditation will occur incrementally throughout IATF development where the stakeholder's objectives for testing or integration will dictate the functionality to be verified and validated.

With respect to the Emulators, the CECB will accredit the integrated simulation as representative of the SLS Block 1 vehicle.

The discussion of re-accreditation resulting from changes to the IATF HWIL Simulation is forward work.

7.0 CERTIFICATION

Facility Certification is described in the SLS IATF Development plan (SLS-PLAN-065) in Section 10.0.

APPENDIX A
ACRONYMS AND ABBREVIATIONS AND GLOSSARY OF TERMS

A1.0 ACRONYMS AND ABBREVIATIONS

A/D	Analog to Digital
AFSW	Avionics and Flight Software
ARTEMIS	Advanced Real-Time Environment for Modeling, Integration, and Simulation
ASSIST	Avionics System Simulation, Integration, and Support Team
BEA	Bilateral Exchange Agreement
BEO	Beyond Earth Orbit
CCB	Configuration Control Board
CDL	Compliance Data List
CECB	Chief Engineer's Control Board
CLE	CSCI Lead Engineer
CM	Configuration Management
COTS	Commercial Off the Shelf
CR	Change Request
CSC	Computer Software Component
CSCI	Computer System/Software Configuration Item
CSU	Computer Software Unit
D/A	Digital to Analog
DAC	Design Analysis Cycle
DBOB	Data Breakout Box
DDT&E	Design, Development, Test, and Evaluation
DLE	Discipline Lead Engineer
DR	Data Requirements
DRD	Data Requirements Description
DRL	Data Requirements List
DVO	Detailed Verification Objective
FQT	Flight Qualification Testing
GN&C	Guidance, Navigation, and Control

GSDOP	Ground Systems Development and Operations Program
GSDOPS	Ground Systems Development and Operations System
HOSC	Huntsville Operations Support Center
HW	Hardware
HWIL	Hardware in the Loop
I/O	Input/Output
IATF	Integrated Avionics Test Facilities
ICPS	Interim Cryogenic Propulsion System
IMACS	Integrated Measurements and Command System
ISPE	Integrated Spacecraft and Payload Element
ITV&V	Integration, Test, Verification, and Validation
LSE	Lead Systems Engineer
M&FM	Mission, and Fault Management
MAESTRO	Managed Automation Environment for Simulation, Test, and Real-Time Operations
MAVRIC	MArshall Vehicle Representation In C
MIL-STD	Military Standard
MPCV	Multi-Purpose Crew Vehicle
MPS	Main Propulsion System
MSFC	Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
NGOs	Needs, Goals, and Objectives
NPR	NASA Procedural Requirements
OPR	Office of Primary Responsibility
OS	Operating System
PBOB	Power Breakout Box
PDR	Preliminary Design Review
POC	Point of Contact
PMTP	Program Master Test Plan
QA	Quality Assurance
ROD	Review of Design
S&MA	Safety and Mission Assurance
SAP	Software Assurance Plan
SCaN	Spacecraft Communications and Navigation
SCR	Software Change Requests
SDL	Software Development Lab

SE	Systems Engineering
SLS	Space Launch System
SLSP	Space Launch System Program
SR&QA	Safety, Reliability and Quality Assurance
SRB	Software Review Board
SME	Subject Matter Expert
SPIO	Spacecraft and Payload Integration Office
SW	Software
TBD	To Be Determined
TBR	To Be Resolved
TRRB	Test Readiness Review Board
UBOB	Umbilical Breakout Box
UUT	Unit Under Test
VA	Verification Acceptance
V&V	Verification and Validation
VCA	Verification Closure Authority
VCR	Verification Closure Report
VTT	Verification Task Team
VV&A	Verification, Validation, and Accreditation

A2.0 GLOSSARY OF TERMS

(Example of Glossary Term)

Term	Description
Flight	The sequence of events that takes place between liftoff and landing of a transportation vehicle.

APPENDIX B
ROLES AND RESPONSIBILITIES

B1.0 ASSIST TEAM V&V ROLES AND RESPONSIBILITIES

Table B1-1. ASSIST Team V&V Roles and Responsibilities Summary

Section	Systems Engineering	ARTEMIS	MAESTRO	Facilities	CM	QA S&MA
4.1	Lead DVO development	Support	Support	Support	Baseline DVOs	Review DVO
4.2	•Test Plans •Test Procedures •Test Report	Support	Support	Support	CM test results & reports	Review and monitor test activities
4.3.	•Test Plans •Test Procedures •Test Report	Support	Support	Support	CM test results & reports	Review and monitor test activities
5.1	Lead	Support	Support	Support	CM Approval	Review
5.2.1	Lead		Support		CM Data	Review
5,2.2	Lead	Support			CM Data	Review
5.3	Lead	Support	Support	Support	CM Data	Review

B2.0 EXTERNAL V&V DEPENDENCIES

Table B2-1. External V&V Dependencies

Organization	Verification Support	Validation Support
SLS Systems Engineering	• Provide SLS design scenarios to be used for evaluating the performance of the integrated • Provide High-fidelity models related to non-element or vehicle-wide features and V&V data in accordance with SLS Development Plan (SLS-PLAN-065) Table C-1. • SME support for each internally developed model. - Review and approve IATF model DVO	• SME support for each internally developed model. - Provide comparison validation data for a given set of agreed-to inputs - Review comparison results and approve model for each specific test purpose • SME support of IATF HWIL Simulation - Review and approve model DVO - Provide comparison validation data for a given set of agreed-to inputs - Review comparison results and approve

Organization	Verification Support	Validation Support
	• SME support of IATF HWIL Simulation - Review and approve IATF model DVO	model for each specific test purpose
SLS Chief Engineer	TBD	TBD
SLS Booster Element	• *Provide SLS models and V&V data in accordance with SLS Development Plan (SLS-PLAN-065) Table C-1. Review and approve IATF model DVOs	• SME support for each externally provided model. - Provide comparison validation data for a given set of agreed-to inputs - Review comparison results and approve model for each specific test purpose
SLS Core Prime	• *Provide SLS models and V&V data in accordance with SLS Development Plan (SLS-PLAN-065) Table C-1. - Review and approve IATF model DVOs	• SME support for each externally provided model. - Provide comparison validation data for a given set of agreed-to inputs - Review comparison results and approve model for each specific test purpose
SLS Engine Element	• *Provide SLS models and V&V data in accordance with SLS Development Plan (SLS-PLAN-065) Table C-1. - Review and approve IATF model DVOs	• SME support for each externally provided model. - Provide comparison validation data for a given set of agreed-to inputs - Review comparison results and approve model for each specific test purpose
SLS Flight Software	TBD	TBD
HOSC	• Provide ESF Appliance and data archive verification data report - Review and approve associated IATF DVOs	TBD
MPCV	TBD	TBD
GSDOP	TBD	TBD
IMACS Team	TBD	TBD

* These model deliveries and support are included in the prime contractor statement of work and respective DRD.

APPENDIX C
VV&A ARTIFACTS

C1.0 IATF V&V ARTIFACTS

As each V&V task is completed, the IATF team will generate artifacts associated with the task. Table 2 provides a description of each artifact and responsible organization(s)

Table C1-1. V&V ARTIFACTS AND Responsibility

V&V Artifact	Description	Responsible Organization
SW Version Description Document (VDD)	VDD for both system CSCIs (ARTEMIS and MAESTRO)	TBD
Requirement Verification Matrix	Matrix of requirements implemented and status of verification performed	TBD
Traceability matrix	Matrix of bi-directional trace of SLS SIL, CSCI requirements, and HW	TBD
System Integration Test Result Report	SLS SIL System Level Testing that includes SW, HW, and all CIs defined for facility configuration	TBD
Test Plan and Procedures	SLS SIL CSCI System-Level test plan and procedures executed for this delivery	TBD
Development Metric Summary	Product and process metric. Product metrics that address maturity, management and lifecycle. Process metrics will address as warranted size, architecture, structure, quality and complexity *	TBD
Physical Configuration Audit (PCA)	The formal examination of the as-built configuration item against its as-designed documentation.	TBD
Functional Configuration Audit (FCA)	The formal examination of functional characteristics of a configuration item, prior to acceptance, to verify that the item has achieved the performance specified in the functional and developmental baseline identification documentation	TBD
Safety Assessment	S&MA Audit Report	TBD
Full Facility System Dry Run Test Results	Comprehensive integration test of facility configuration	TBD

APPENDIX D
OPEN WORK

All resolved TBDs, TBRs, and forward work items should be listed on the Change Request (CR) the next time the document is updated and submitted for formal review, and that will serve as the formal change record through the configuration management system.

D1.0 TO BE DETERMINED

Table D1-1 lists the specific To Be Determined (TBD) items in the document that are not yet known. The TBD is inserted as a placeholder wherever the required data is needed and is formatted in bold type within carets. The TBD item is sequentially numbered as applicable (i.e., **<TBD-001>** is the first undetermined item assigned in the document). As each TBD is resolved, the updated text is inserted in each place that the TBD appears in the document and the item is removed from this table. As new TBD items are assigned, they will be added to this list in accordance with the above-described numbering scheme. Original TBDs will not be renumbered.

Table D1-1. To Be Determined Items

TBD	Section	Description
TBD-001	4.2.2	Guidance for Problem Reports
TBD-002	4.3.1	Table 4-2 completion
TBD-003	4.3.2.2	Table 4-3 completion
TBD-004	4.3.2.3	Table 4-4 completion
TBD-005	4.3.3.2	Table 4-5 completion
TBD-006	4.3.3.2	Table 4-6 completion
TBD-007	4.3.3.3	Table 4-7 completion
TBD-008	4.3.4	Emulator documentation required for delivery
TBD-009	Table B2-1	External V&V Dependencies
TBD-010	Table C1-1	Assignment of responsibilities to the products identified

D2.0 TO BE RESOLVED

Table D2-1 lists the specific To Be Resolved (TBR) issues in the document that are not yet known. The TBR is inserted as a placeholder wherever the required data is needed and is formatted in bold type within carets. The TBR issue is sequentially numbered as applicable (i.e., **<TBR-001>** is the first unresolved issue assigned in the document). As each TBR is resolved, the updated text is inserted in each place that the TBR appears in the document and the issue is removed from this table. As new TBR issues are assigned, they will be added to this list in accordance with the above-described numbering scheme. Original TBRs will not be renumbered.

Table D2-1. To Be Resolved Issues

TBR	Section	Description
TBR-001		

D3.0 FORWARD WORK

Table D3-1 lists the specific forward work items identified during this document's Change Request (CR) review and evaluation. Each item is given a sequential number using a similar format to that for the TBDs and TBRs. For each item, include the section number(s) of this document that the open work will impact, and in the Description include the specific number of the comment from the Change Evaluation (CE), i.e., CE-10, CE-27. Do not include a placeholder for forward work items in the body of the document; list them only in Table D3-1.

Table D3-1. Forward Work

FWD	Section	Description
FWD-001	1.0	May need to discuss the need for external emulators
FWD-002	1.1	Need to add a reference to the SLS-PLN-173 SLP M&S Plan and/or the SLS SW Management plan
FWD-003	4.3.4	Describe the Process of release and deployment of the emulators
FWD-004	5.0	Need to describe the role f QA and S&MA in validation
FWD-005	5.0	Need to connect to section C.2.4 Product Validation Process out of the NPR 7123.1A. Specifically how will acceptability criteria will be specified
FWD-006	5.2.2	Need to reference SME commitments with the SE&I PAD agreements
FWD-007	6.0	Need to address re-accreditation when changes are made
FWD-008	7.0	Need to address re-certification when changes are made
FWD-009	4.2	Too much common wording among sub-sections, consider revising to clarify and make unique
FWD-010	4.1	This section will need to be expanded to describe what a DVO is, how it will be developed, who will be involved.
FWD-011	Table B2-1	This table needs to be completed and specific dependencies identified
FWD-012	Table C1-1	This table needs to be completed and specific products identified
FWD-013	4.3.4	Need to describe the verification of the delivered emulators provided by MPCV and GSDOP